B.Tech III Year II Semester (R09) Supplementary Examinations December/January 2014/2015
**VLSI DESIGN**
(Common to ECE, EIE and E.Con.E)

Time: 3 hours

Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
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1      With neat sketches explain oxidation process in IC fabrication.

2  (a)  Write clearly about design hierarchy.
   (b)  Explain the concepts of regularity, modularity and locality.

3      Draw the CMOS NOR gate & its physical layout with stick diagram.

4  (a)  What are the two basic forms of interconnection trees? What are the two wiring models of an interconnect? Explain them.
   (b)  Estimate the interconnect delay using Van Ginneken algorithm.

5  (a)  Implement a 8-bit comparator using 4-bit comparators and other interfacing requirements.
   (b)  With the help of logic diagram explain the working of 4-bit comparator.

6      Implement the following using gate logic, switch logic and PLA in NMOS:
       (i) 4:1 multiplexer.  (ii) 4-bit comparator.  (iii) 8-bit parity generator.

7  (a)  Explain register transfer level synthesis.
   (b)  With the help of an example explain how designing is optimized at register transfer level.

8  (a)  Explain about IDDQ ($V_{DD}$ supply current quiescent) testing for bridging faults?
   (b)  Explain how a Pseudo random sequence generator and a signature analyzer is used to test an 8-input combinational circuit.

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